INTEGRATED CIRCUITS EQUIVALENTS LIST

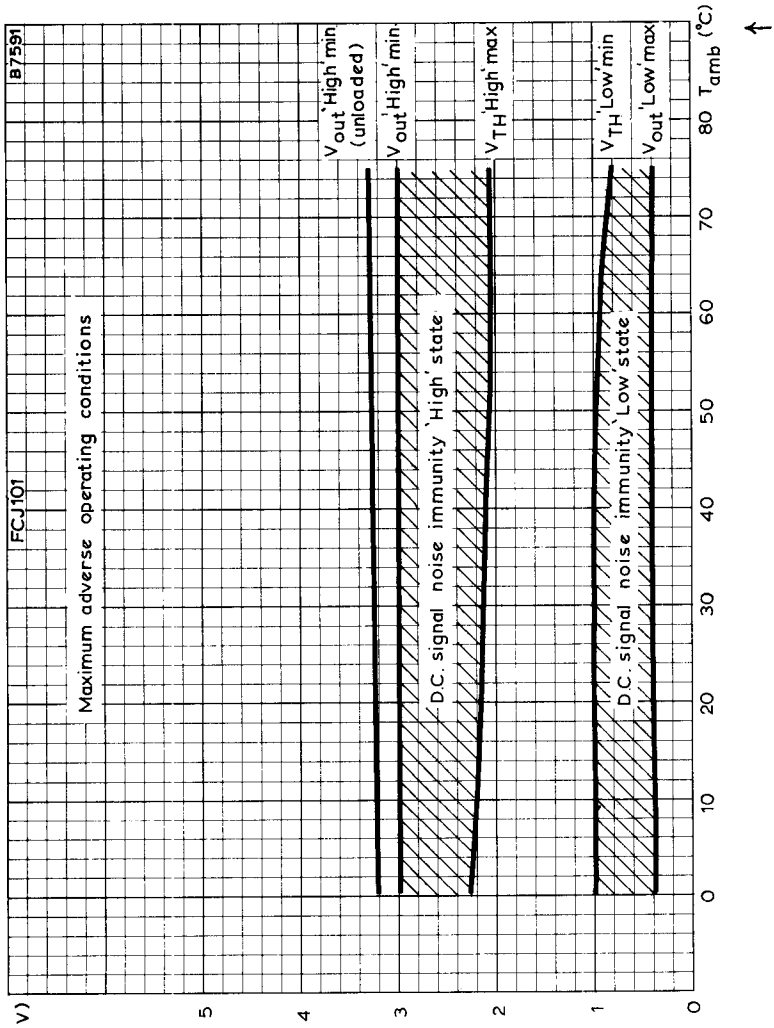
COMMERCIAL VERSIONS

Type No.	*Mullard equivalent*	*Type No.*	*Mullard comparable types*
DTL range		**TTL range**	
– RC 206	FCH 141	7400N	FJH131
	FCL 101	7401N	FJH231
– RC 210	FCH 221	7402N	FJH221
– RC 216	FCH 151	7410N	FJH121
	FCK 101	7420N	FJH111
– RC 224	FCH 101	7430N	FJH101
– RC 225	FCJ 101	7440N	FJH141
– RC 226	FCH 161	7441AN	FJL101
– RC 227	FCY 101	7450N	FJH151
– RC 231	FCH 121	7451N	FJH161
– RC 234	FCH 111	7453N	FJH171
– RC 236	FCH 171	7460N	FJY101
– RC 246	FCH 181	7470N	FJJ101
– RC 261	FCH 131	7472N	FJJ111
– RC 266	FCH 191	7473N	FJJ121
– RC 286	FCH 201	7474N	FJJ131
– RC 296	FCH 211	7475N	FJJ181
		7476N	FJJ191
		7490N	FJJ141

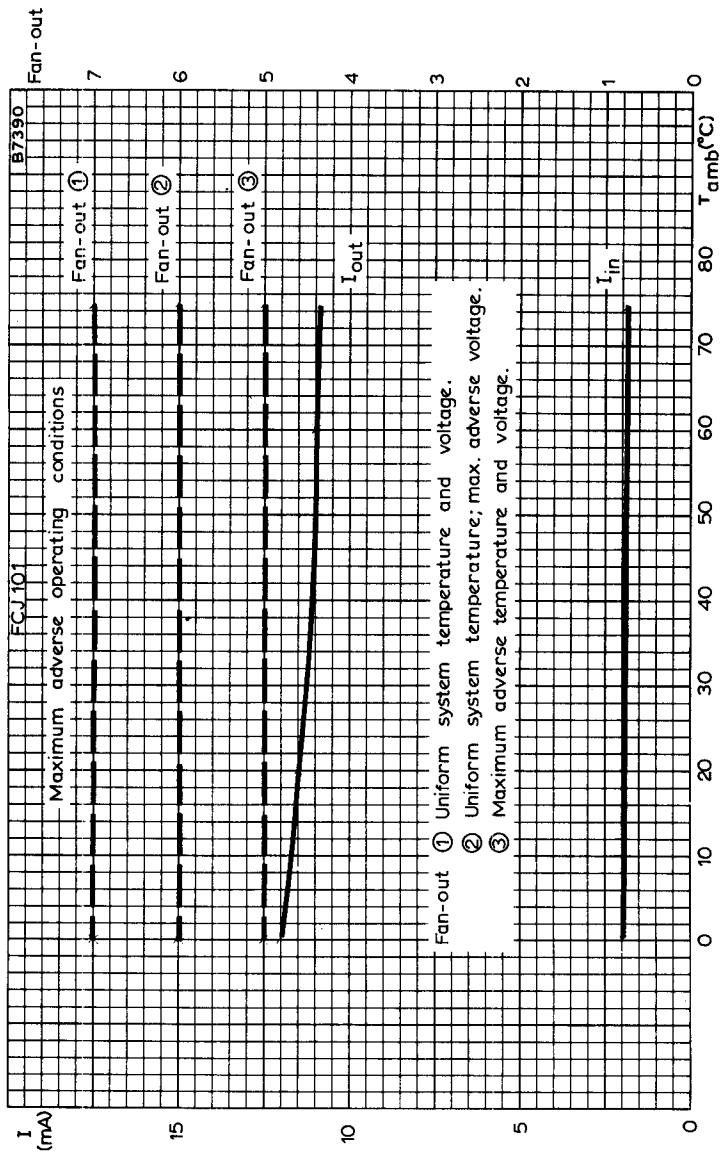
MILITARY VERSIONS

DTL range

Type No.	*Mullard equivalent*	*Type No.*	*Mullard equivalent*
		– RM 227	FCY 102
– RM 206	FCH 142	– RM 231	FCH 122
	FCL 102	– RM 210	FCH 112
– RM 210	FCH 222	– RM 236	FCH 172
– RM 216	FCH 152	– RM 246	FCH 182
	FCK 102	– RM 261	FCH 132
– RM 224	FCH 102	– RM 266	FCH 192
– RM 225	FCJ 102	– RM 286	FCH 202
– RM 226	FCH 162	– RM 296	FCH 212



DESIGN CURVE
VARIATION OF D.C. LEVELS WITH AMBIENT TEMPERATURE



DESIGN CURVE
VARIATION OF FAN-OUT WITH AMBIENT TEMPERATURE
VARIATION OF OUTPUT AND INPUT CURRENTS WITH AMBIENT TEMPERATURE

JK FLIP-FLOP FCJ101

TENTATIVE DATA

The FCJ101 is a monolithic diode-transistor logic JK flip-flop. The state of the flip-flop can be changed by a 'Low' signal at the SET inputs, regardless of the state of the TRIGGER input.

QUICK REFERENCE DATA		
Supply voltage (nominal)	+6.0	V
Operating temperature range	0 to +75	^{o}C
Number of J and K inputs (each)	3	
Number of SET inputs (each)	1	
Fan-out capability at 25°C (to FCH gate and J or K inputs)	7	
Signal noise immunity ('Low') at 25°C (typ.)	1.2	V
Maximum operating frequency at 25°C	5.0	MHz
Average power dissipation (max.) (50% duty cycle, T_{amb} = 25°C	81	mW

OUTLINE

14-lead dual in-line package
For details see General Explanatory Notes

LOGIC FUNCTION

When the SET inputs are 'High' and the J and K inputs are 'High' the output changes state every time the clock pulse is applied.

When the SET inputs are 'High' and one or more of the J inputs and one or more of the K inputs are 'Low' then the output states are unchanged by the application of the clock pulse.

When the SET inputs are 'High' and all of the J inputs are 'High' and one or more of the K inputs are 'Low' then after the clock pulse, output 1 is 'Low' and output 2 is 'High' and vice versa.

When the SET input is 'Low' then the associated output is 'High'.

When both SET inputs are 'Low' then the outputs are 'High' until the SET inputs go 'High' when the state of the bistable becomes indeterminate.

DESIGN DATA

Over the full temperature range 0 to 75°C

	Min.	Nom.	Max.	
Supply				
Supply voltage	5.7	6.0	6.3	V
Current consumption from supply				
Clock terminal 'Low' V supply = 6.0V	-	7.5	-	mA
V supply = 6.3V	-	-	13.3	mA
Clock terminal 'High' V supply = 6.0V	-	7.0	-	mA
V supply = 6.3V	-	-	12.3	mA

Input

Data can be read into the J-K terminals with the clock in either the 'Low' state or the 'High' state. A change from 'Low' to 'High' at the J or K inputs must occur typically 15ns before the clock pulse goes negative in order to set the flip-flop to a different state. A change from 'High' to 'Low' must occur typically 35ns before the clock pulse goes negative in order to set the flip-flop to a different state.

Voltage for 'High' input state S.N.I. = 0	2.3	-	6.3	V
S.N.I. = 0.7V	3.0	-	6.3	V←
Current for 'High' input state	-	-	30	μA
Voltage for 'Low' input state S.N.I. = 0	-	-	0.8	V
S.N.I. = 0.4V	-	-	0.4	V
Current for 'Low' input state (full temperature range, see curve on page C2 for other temperatures)				
J and K inputs	-	-	2.0	mA
SET inputs	-	-	4.0	mA
Clock input (peak)	-	-	4.0	mA

Clock input

This flip-flop switches when the negative going portion of the clock waveform crosses a threshold in the region of +1.6 to 1.0V. The clock waveform should have a fall time no greater than 0.1μs for general applications, and need only be in the 'High' state for 25ns.

Output

Voltage for 'High' output state	3.0	-	6.3	V←
Voltage for 'Low' output state	-	-	0.4	V
Current capability at 'Low' output state (T_{amb} = 75°C, see curve on page C2 for other temperatures)	-	-	10.8	mA
D.C. Fan-out to J or K inputs or gate inputs*				
1. Uniform system temperature and voltage	-	-	7	
2. Uniform system temperature, adjacent circuits at extremes of supply voltage	-	-	6	
3. Adjacent circuits at extremes of temperature and supply voltage.	-	-	5	

*Fan-out is halved to SET or Clock inputs.

DESIGN DATA (cont'd)

Truth tables

SET input terminals

SET input 1	SET input 2	Output 1	Output 2
Low	Low	High*	High*
Low	High	High	Low
High	Low	Low	High
High	High	No change	No change

*The output will become indeterminate when the SET inputs go 'High'.

JK input terminals (output signal after complete trigger pulse, SET input terminals in 'High' state).

J input	K input	Output 1	Output 2
Low	Low	No change	No change
Low	High	High	Low
High	Low	Low	High
High	High	Reversed	Reversed

PERFORMANCE

SET input signal noise immunity

	Min.	Nom.	Max.	
'Low' state	400	-	-	mV
'High' state	0.7	-	-	V←
Counting rate (Fan-out=1, C_L=25pF)	-	-	5.0	MHz

CHARACTERISTICS (Supply voltage=+6.0V, T_{amb}=25°C)

		Min.	Typ.	Max.	
V_{TH} 'Low'	SET input threshold voltage for 'Low' input state (other SET input at 0V, V_{out}=3.2V, J and K input o/c, R_L=1MΩ)	1.0*	-	-	V
V_{TH} 'High'	SET input threshold voltage for 'High' input state (other SET input at 0V, I_{out}=12.6mA, J and K inputs o/c)	-	-	2.2*	V
V_{out} 'Low'	Voltage for 'Low' output state (V_{in}=2.2V, I_{out}=12.6mA)	-	-	0.4*	V

CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
I_{in} 'High'	Input current for 'High' input state SET, J or K inputs (V_{in} = 6.0V, all other inputs at 0V)	-	-	25	μA
	Clock input	-	-	5.0	μA
I_{in} 'Low'	Input current for 'Low' input state SET inputs (V_{in} = 0.4V, other inputs at 6.0V)	-	-	3.6*	mA
	J, K and Clock inputs	-	-	1.8*	mA

*These are the characteristics which are recommended for acceptance testing purposes.

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

Maximum positive supply voltage (pin 7)	8.0	V
Maximum positive output voltage (pins 5 and 10)	7.0	V
Maximum negative output voltage	0	V
Maximum positive voltage on inputs (pins 1, 2, 3, 4, 6, 9, 11, 12, 13)	7.0	V
Maximum negative voltage on inputs	0	V

Temperature

T_{stg} min.	-35	°C
T_{stg} max.	125	°C
T_{amb} min. operating	0	°C
T_{amb} max. operating	75	°C

PINNING

1.	J1 input	8.	I.C.
2.	J3 input	9.	S2 SET input
3.	T trigger input	10.	Q2 output
4.	J5 input	11.	K2 input
5.	Q1 output	12.	K4 input
6.	S1 SET input	13.	K6 input
7.	Positive supply	14.	Common and earth

CIRCUIT DIAGRAM