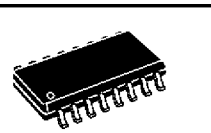
SGS-THOMSON MICROELECTRONICS

L6574

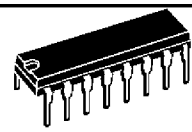
CFL/TL BALLAST DRIVER PREHEAT AND DIMMING

PRODUCT PREVIEW

- HIGH VOLTAGE RAIL UP TO 600V
- dV/dt IMMUNITY ± 50 V/ns IN FULL TEMPERATURE RANGE
- DRIVER CURRENT CAPABILITY:
  250mMA SOURCE
  450mA SINK
- SWITCHING TIMES 80/40ns RISE/FALL WITH 1nF LOAD
- CMOS SHUT DOWN INPUT
- UNDER VOLTAGE LOCK OUT
- PREHEAT AND FREQUENCY SHIFTING TIMING
- SENSE OP AMP FOR CLOSED LOOP CONTROL OR PROTECTION FEATURES
- HIGH ACCURACY CURRENT CONTROLLED OSCILLATOR
- INTEGRATED BOOTSTRAP DIODE
- CLAMPING ON Vs.
- SO16, DIP 16 PACKAGE



SO16N



DIP16

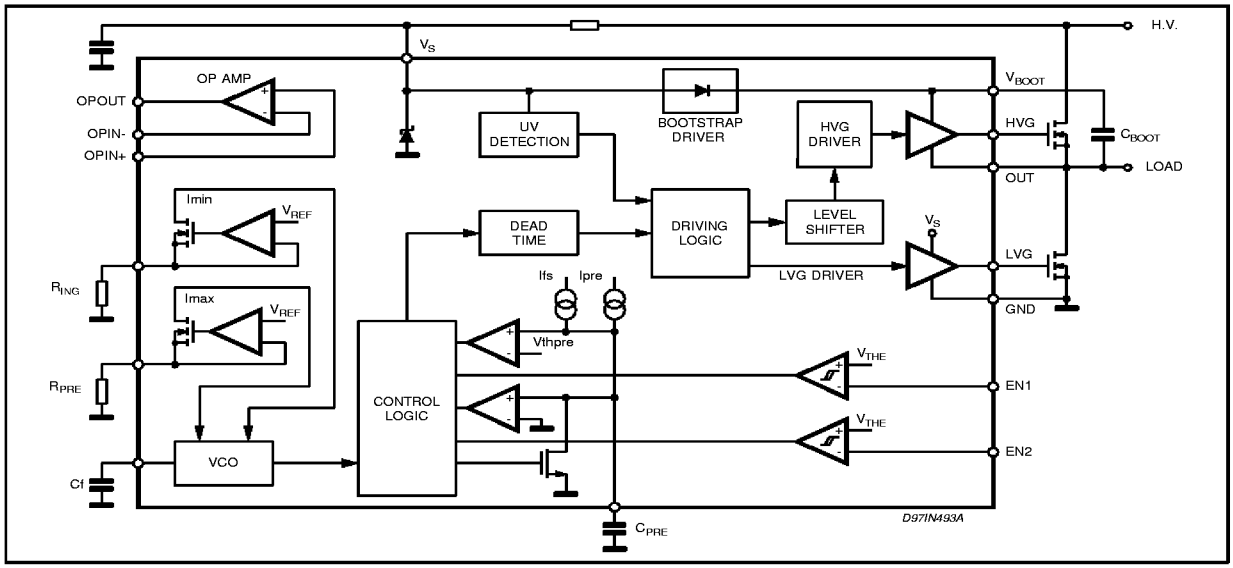
ORDERING NUMBERS:

L6574D L6574

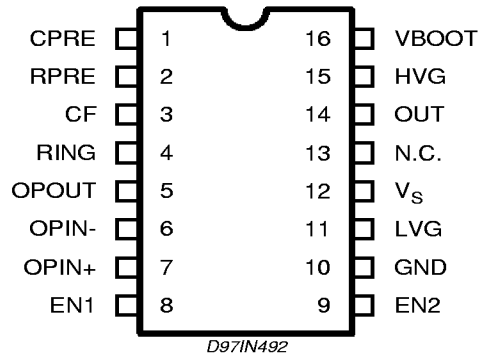
DESCRIPTION

The L6574 is manufactured with the BCD OFF LINE technology, able to ensure voltage ratings in excess of 600V, making it perfectly suited for ballast driver application.
The device is intended to drive two Power MOS, in the classical Half Bridge Topology, ensuring all the features needed to drive and control properly a fluorescent bulb.
Thanks to a dedicated Timing Section, the L6574 let the user set at his ease, the parameter for a proper Pre-Heat/Ignition of the lamp.
Also an OP AMP is available to implement a Closed Loop control of Lamp Current during normal Lamp Burning.
Dimming can be easily performed thanks to a VCO input.
An integrated Bootstrap Section, saving the normally required bootstrap diode and the zener clamping on Vs, make the L6574 perfectly fitting also in Low Cost applications as very few spare parts around are needed to built an high performance ballast driver.

BLOCK DIAGRAM



PIN CONNECTION



THERMAL DATA

Symbol	Parameter	DIP16	SO16N	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to ambient Max.			°C/W

PINS DESCRIPTION

N.	Name	Function
1	Cpre	Preheat Timing Capacitor
2	Rpre	Maximum Oscillation Frequency Setting. Low Impedence Voltage Source. See also Cf
3	Cf	Oscillator Frequency Setting (see also Ring, Rpre)
4	Ring	Minimum Oscillation Frequency Setting. Low Impedence Voltage Source. See also Cf
5	OPout	Sense OP AMP Output. Low Impedence
6	OPin-	Sense OP Amp Inverting Input. High Impedence
7	OPin+	Sense OP AMP Non Inverting Input High Impedence.
8	EN1	Half Bridge Enable
9	EN2	Half Bridge Enable
10	GND	Ground
11	LVG	Low Side Driver Output
12	Vs	Supply Voltage with Internal Zener Clamp.
13	N.C.	Non Connected
14	OUT	High Side Driver Reference
15	HVG	High Side Driver Output
16	Vboot	Bootstrapped Supply Voltage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
I_S	Supply Current (*)	25	mA
V_{LVG}	Low Side Output	-0.3 to Vs +0.3	V
V_{OUT}	High Side Reference	-1 to VBOOT -18	V
V_{HVG}	High Side Output	-1 to VBOOT	V
V_{BOOT}	Floating Supply Voltage	-1 to 618	V
dV_{BOOT}/dt	V_{BOOT} pin Slew rate (repetitive)	±50	V/ns
dV_{OUT}/dt	OUT pin Slew Rate (repetitive)	±50	V/ns
V_{ir}	Forced Input Voltage (pins Ring, Rpre)	-0.3 to 5	V
V_{ic}	Forced Input Voltage (pins Cpre, Cf)	-0.3 to 5	V
V_{opc}	Sense Op Amp Common Mode Range	-0.3 to 5	V
V_{opd}	Sense Op Amp Differential Mode Range	±5	V
V_{opo}	Sense Op Amp Output Voltage (forced)	4.6	V
T_{stg}, T_j	Storage Temperature	-40 to +150	°C
T_{amb}	Ambient Temperature	-40 to +125	°C

(*) The device has an internal Clamping Zener between GND and the Vcc pin, it must not be supplied by a Low Impedance Voltage Source.
Note: ESD immunity for pins14, 15 and 16 is guaranteed up to 900V (Human Body Model)

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	10 to V_{CL}	V
V_{OUT} (*)	High Side Reference	-1 to V_{BOOT}-V_{CL}	V
V_{BOOT} (*)	Floating Supply Voltage	500	V

(*) If the condition Vboot - Vout < 18 is guaranteed, Vout can range from -3 to 580V.

ELECTRICAL CHARACTERISTICS (V_S = 12V; V_{BOOT}-V_{OUT} = 12V; T_{amb} = 25°C)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage							
V_{suvp}	12	V_s Turn On Threshold		9.5	10.2	10.9	V
V_{suvn}		V_s Turn Off Threshold		7.3	8	8.7	V
V_{suvh}		Supply Voltage Under Voltage Hysteresys			2.2		V
V_{cl}		Supply Voltage Clamping		14.6	15.6	16.6	V
I_{su}		Start Up Current	$V_S < V_{suvn}$			250	µA
I_q		Quiescent Current, fout = 60kHz, no load.	Vs > V_{supv}		2		mA
High voltage Section							
$I_{bootleak}$	16	BOOT pin leakage current	V_{BOOT} = 580V			5	µA
$I_{outleak}$	14	OUT pin Leakage Current	V_{OUT} = 562V			5	µA
High/Low Side Drivers							
I_{hvgso}	15	High Side Driver Source Current	V_{HVG}-V_{OUT} = 0	170	250		mA
I_{hvgsi}	15	High Side Driver Sink Current	V_{HVG}-V_{BOOT} = 0	300	450		mA
I_{hvgso}	11	Low Side Drive Source Current	VLVG-GND	170	250		mA
I_{lvgsi}	11	Low Side Drive Source Current	V_{LVG}-V_S = 0	300	450		mA
t_{rise}	15, 11	Low/High Side Output Rise Time	C_{load} = 1nF		80	120	ns
t_{fall}		Low/High Side Output Fall Time	C_{load} = 1nF		50	80	ns

ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Pin	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Oscillator							
D_C	14	Output Duty Cycle		48	50	52	%
f_{ing}		Minimum Output Oscillation Frequency	C_F = 470pF; R_{ing} = 50k	58.2	60	61.8	kHz
f_{pre}		Maximum Output Oscillation Frequency	C_F = 470pF; R_{ing} = 50k; R_{pre} = 47k	114	120	126	kHz
V_{ref}	1,2	Voltage to current converters threshold			2		V
t_d	12	Dead Time between Low and High Side Conduction		0.8	1.25	1.7	µs
Timing Section							
k_{pre}	4	Pre Heat Timing constant	C_{pre} = 330nF	1	1.5	2	sec/µF
K_{fs}		Frequency Shift Timing Constant	C_{pre} = 330nF	0.1	0.15	0.2	sec/µF
V_{thpre}		Pre Heat Timing Comparator Threshold		3.1	3.5	3.9	V
Sense OP AMP							
I_{ib}	6,7	Input Bias current				0.1	µA
V_{io}		Input Offset Voltage		-10		10	mV
R_{in}		Input Resistance			Tbd		kΩ
R_{out}	5	Ouput Resistance				100	Ω
I_{out}		Output Current				2	mA
I_{out+}		Sink Output Current	V_{out} = 0.2V	0.5			mA
I_{out-}		Source Output Current	V_{out} = 4.5V	0.5			mA
V_{ic}	6,7	Common Mode Input Range		-0.2		3	V
GBW		Sense Op Amp Gain Band Width Product			1		MHz
Gdc		DC Open Loop Gain			80		dB
Comparators							
V_{the}	8,9	Enabling Comparators Threshold		0.56	0.6	0.64	V
V_{hye}		Enabling Comparators Hysteresis		30		90	mV
t_{pulse}		Minimum Pulse lenght			200		ns

High/Low Side driving section:

An High and Low Side driving Section provide the proper driving to the external Power MOS. An high sink/source driving current (450/250 mA typ) ensure fast switching times also when size4 Power MOS need to be driven.

Bootstrap Section:

A patended integrated Bootstrap Section replaces the external Bootstrap Diode needed, together with a Bootstrap Capacitor, to make available the Bootstrapped Voltage needed to drive the High Side PMOS. The fuction is achieved using an High Voltage DMOS, driven synchronous with the Low Side external Power MOS. Current flow into the Vboot pin is inhibited , for a safe operation even when a ZVS operation is not ensured.

Timing Section:

A capacitor connected to pin Cpre, is charged with a fixed current, to set the proper Pre-Heat Time (**tpre=kpre*Cpre**) for the bulb. During tpre, the output is switching at **fpre** (see Oscillator Section). When the tpre is expired, the Cpre capacitor is discharged first and then charged with a different current, to set a second time interval **tsh** (0.1 times the selected Pre-Heat Time tpre) during wich a frequency shifting from fpre to **fing** is performed to ensure lamp ignition.

Oscillator Section:

A Voltage Controlled Oscillator, is responsible to drive, with the selected frequency, the Output Half Bridge. Two frequencies can be indipendently selected:

fpre, effective during tpre, and **fing** effective during normal lamp burning, when working Open Loop, fpre and fing can be considered as, respectively, the highets and the lowest allowed oscillation frequency when the Closed loop operation is considered.

Around the L6574 a closed loop can be implemented to control, by means of adjusting the Oscillation Frequency, the Lamp Current during normal lamp burning. For this purpose the OP AMP Output (see OP AMP Section) can be properly presented at the **Ring** pin.

OP AMP Section:

The integrated OP AMP is designed to offer Low Output Impedence, wide band, High input Impedance and wide Common Mode Range. It can be readily used to implement a Closed Loop Control (see Oscillator Section), of the Lamp Current.

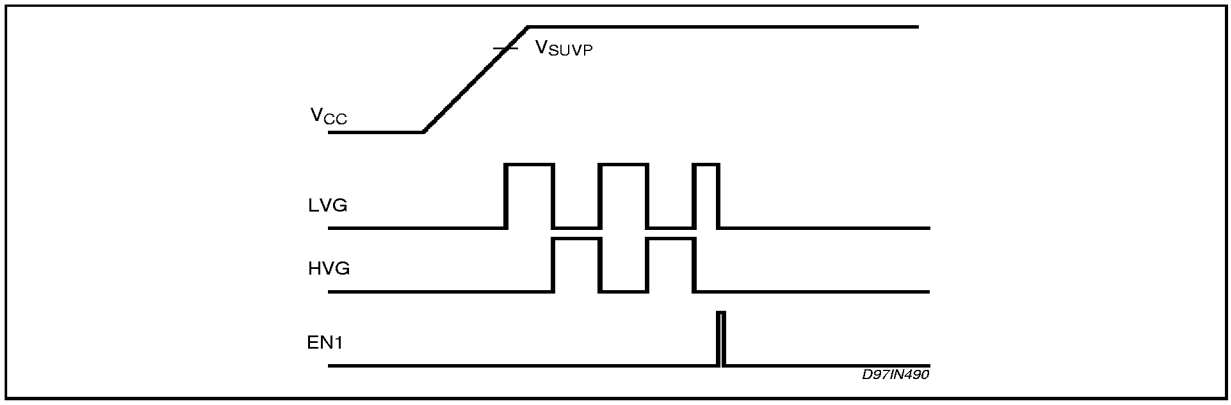
EN1, EN2 Comparators:

Two CMOS comparators, with a threshold set at 0.6 V (typical value), are available to perform protection schemes (e.g. Over Voltage, lamp removal etc.). Short pulses (≥200nsec) on Comparators Input are recognized.

The EN1 input (active High) forces the L6574 in the shut down state (e.g. LVG Low, HVG low, Oscillator stopped), as in the Under Voltage Conditions. Normal Operating conditions are resumed after a power-off power-on sequence, or when EN2 input is high.

The EN2 input (active high) also restarts a preheat sequence (see Timing Diagrams).

TIMING DIAGRAMS



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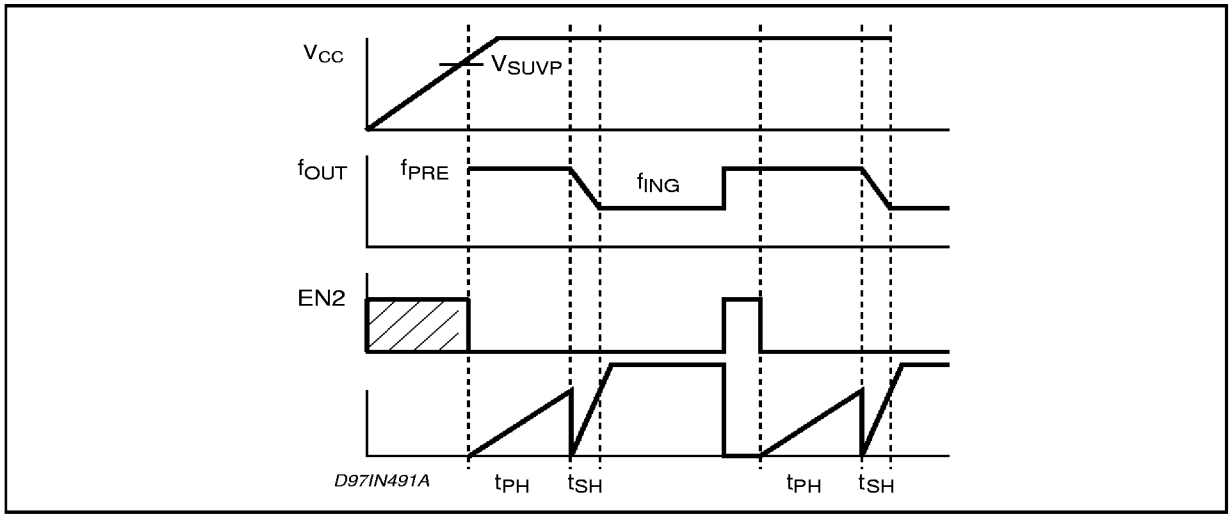

SO16 NARROW PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.069
a1	0.1		0.25	0.004		0.009
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D	9.8		10	0.386		0.394
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.150		0.050
M			0.62			0.024
S	8° (max.)